CLAIMS

1. A resistive structure, integrated in a semiconductor substrate, comprising a suitably doped polysilicon region completely surrounded by a dielectric region, so that the resistive structure is isolated electrically from other components jointly integrated in the semiconductor substrate.

2. The resistive structure of claim 1, wherein portions of the resistive structure are formed with a plurality of trenches having suitable areas and are distributed about the polysilicon region to form a single dielectric region.

3. The resistive structure of claim 1, wherein said polysilicon region and said dielectric region are winding patterns, thereby reducing the space requirements of the resistive structure for a given resistance value.

4. The resistive structure of claim 3, wherein said winding patterns are formed to include rungs, said rungs are connected in parallel together by a metallization.

5. The resistive structure of claim 1, wherein said polysilicon region is masked and then etched to create a T-shaped structure providing connection paths of polysilicon.

6. The resistive structure of claim 1, wherein said polysilicon region comprises fill polysilicon that has been enhanced by implantation in its surface region only.

7. The resistive structure of claim 1, wherein said polysilicon region comprises two deposited layers of undoped polysilicon, only a first of said layers being enhanced by implantation to lower the values of parasitic capacitances associated with the resistive structure.

8. The resistive structure of claim 7, wherein said first polysilicon layer is enhanced by angled implantation and has a thickness dimension conforming to the sidewalls of the dielectric region to prevent said region from becoming filled completely.

9. The resistive structure of claim 1, wherein said semiconductor substrate is a SOI substrate and comprises a plurality of dielectric trenches between wells of integrated devices therein, and that doped polysilicon intended to form the resistive structure is introduced into said trenches, the resistive structure itself requiring no additional integration area.

10. The resistive structure of claim 1, wherein said dielectric region that is arranged to isolate the resistive structure is formed in the process of oxidizing the sidewalls of a dielectric trench.

11. An integrated resistive structure, comprising:

at least one trench having sidewalls formed in a semiconductor substrate;

a dielectric layer entirely coating all walls of the at least one trench; and

a polysilicon region filling the at least one trench to be isolated dielectrically from the semiconductor substrate.

12. The structure of claim 11, wherein the dielectric layer comprises a dielectric oxide formed from oxidizing the walls of the at least one trench.

13. The structure of claim 12, wherein the dielectric layer has vertical and horizontal dimensions that are greater than vertical and horizontal dimensions of the polysilicon region.

14. The structure of claim 11, wherein the polysilicon region has a T-shaped cross-sectional configuration with a stem portion filling the at least one trench and a cap portion

covering the at least one trench and overlapping a portion of a top surface of the silicon substrate on each side of the at least one trench.

15. The structure of claim 11, wherein the polysilicon region includes a doped surface region.

16. The structure of claim 11, wherein the polysilicon region comprises first and second layers of polysilicon, the second layer being undoped and the first layer implanted with a dopant.

17. The structure of claim 16, wherein the first layer of polysilicon is implanted by angled implantation and has a thickness dimension conforming to the walls of the dielectric-coated at least one trench to prevent complete filling of the at least one trench.

18. The substrate of claim 11, comprising a plurality of trenches coupled together electrically by metallization.